Appln. No.: Unknown Docket No.: SNDK.308US0

Title: Non-Volatile Memory and Method With Bit Line to Bit...
Inventors: Cernea et al. Exp. Mail: EV321716430US

Filing Date: Herewith Atty. Tel: (415) 318-1160 Sheet 1 of 16

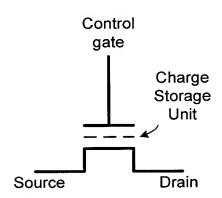


FIG. 1

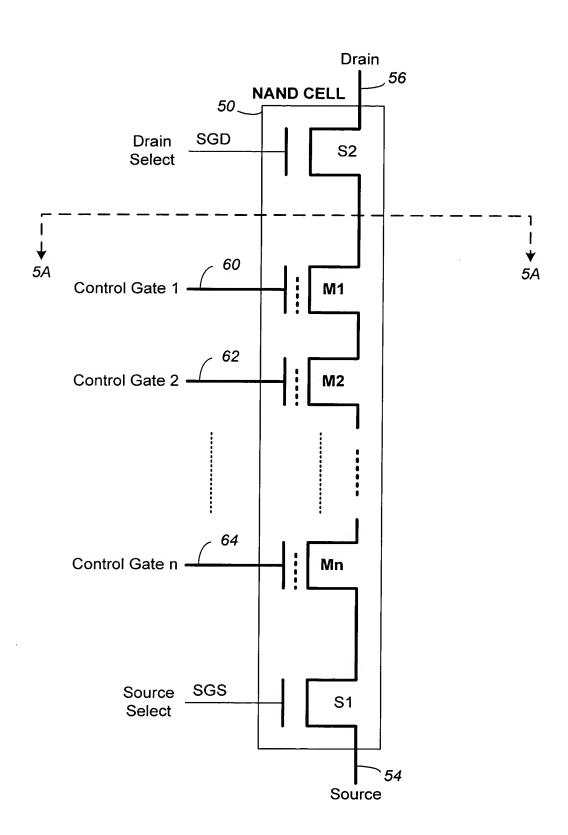


FIG. 2

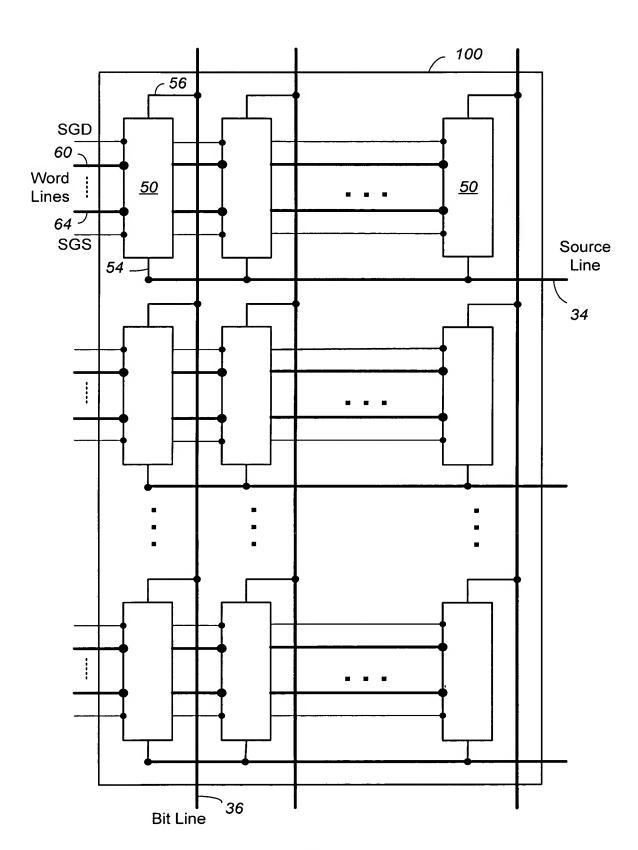


FIG. 3

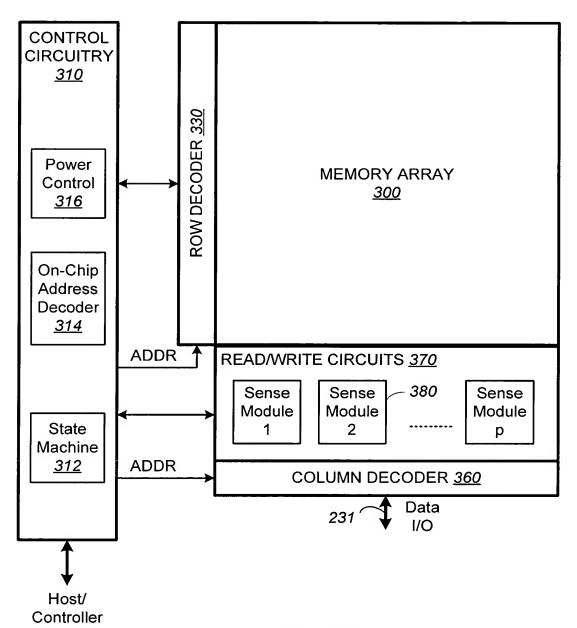


FIG. 4A

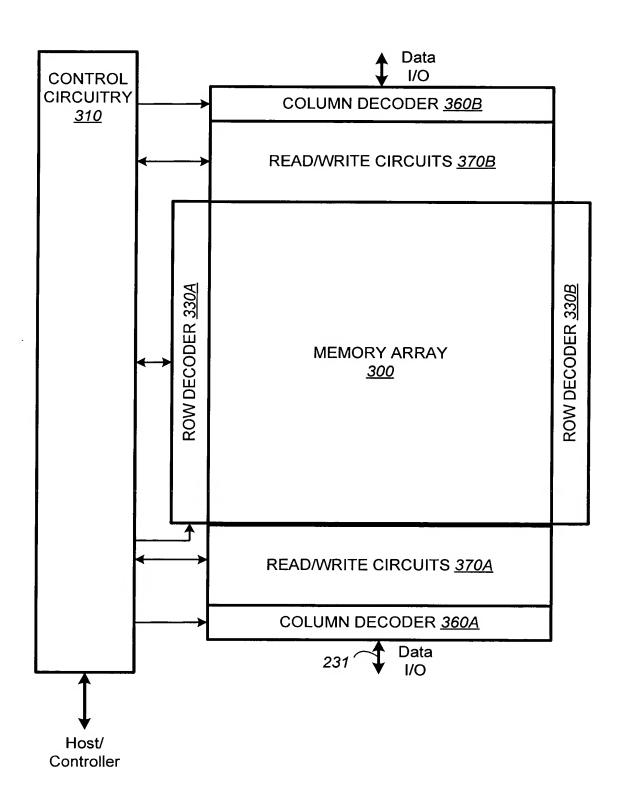


FIG. 4B

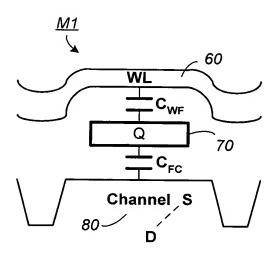


FIG. 5A

$$\begin{array}{c|c} & & & & \\ & & & \\ & & & \\ & & & \\ & & & \\ & & & \\ & & & \\ & & & \\ & & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & & \\ & \\ & & \\ & & \\ & \\ & & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ & \\ &$$

FIG. 5B

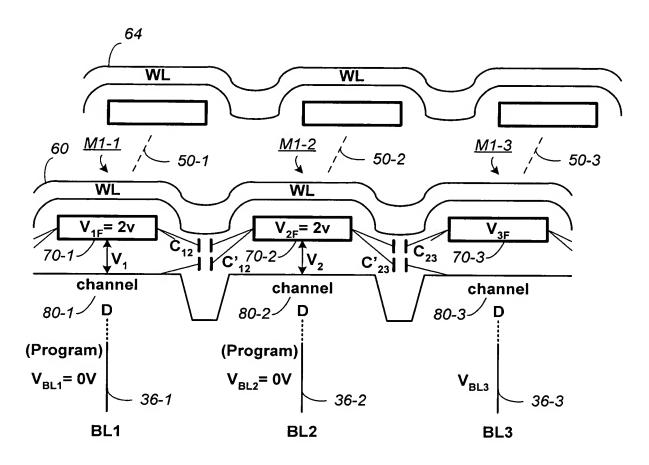


FIG. 6A

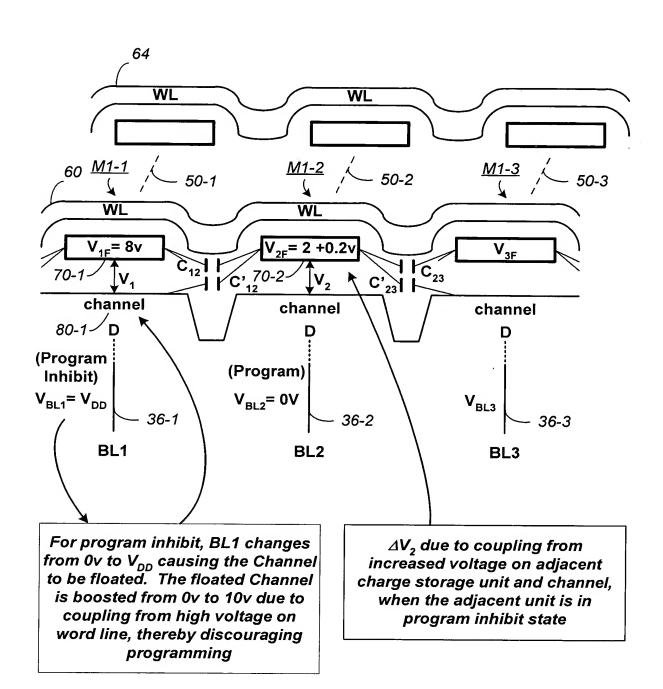


FIG. 6B

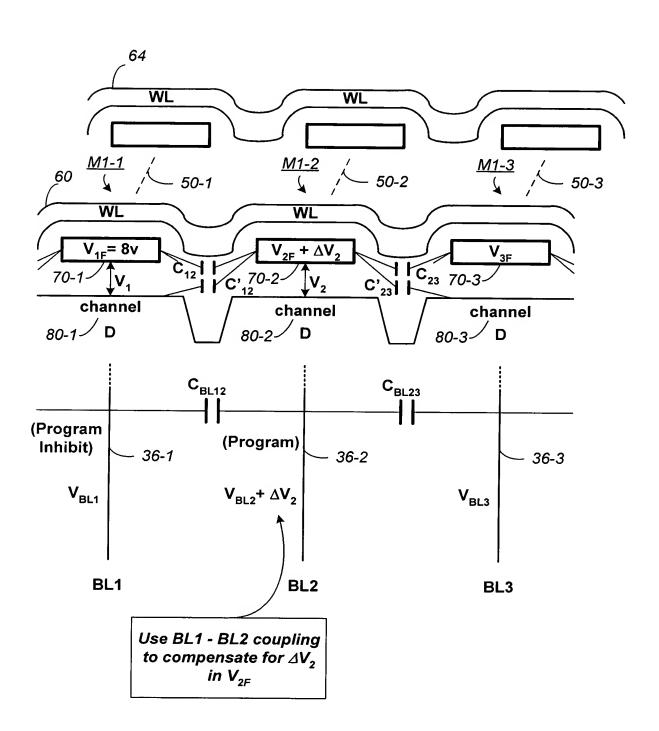


FIG. 7

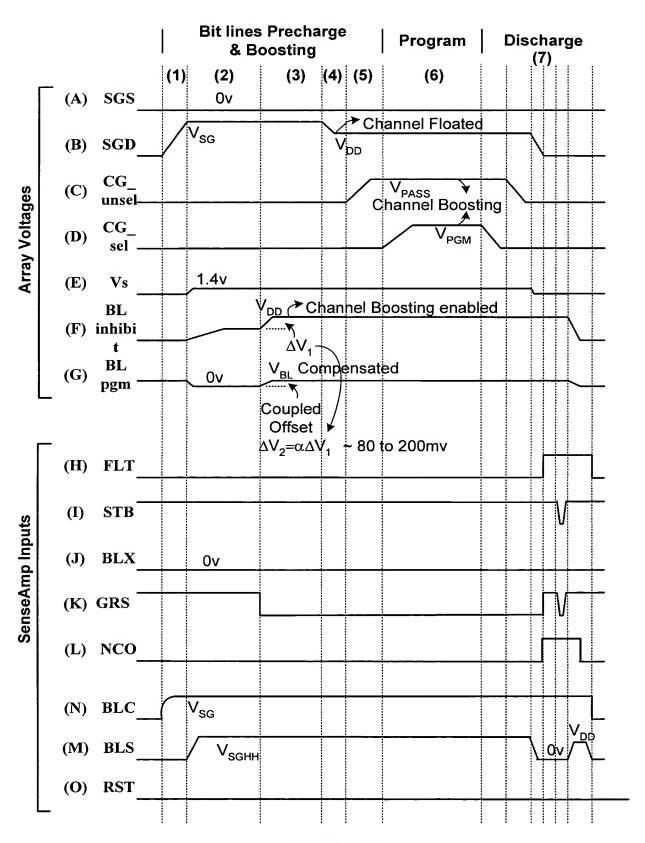


FIG. 8

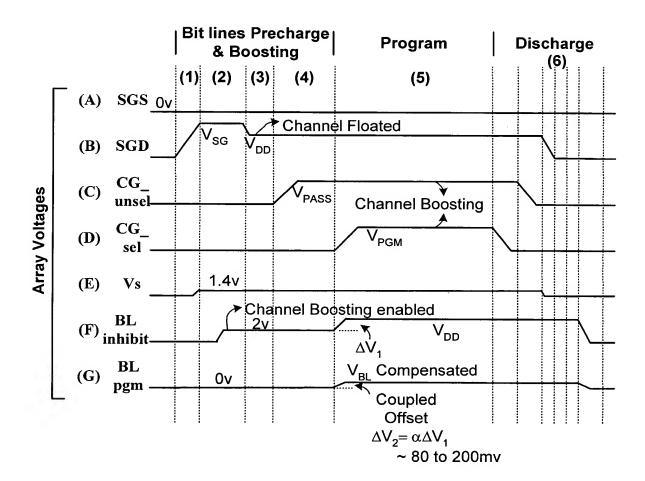


FIG. 9

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All-bit Programming For a page of contiguous memory storage units, each unit having a 400 charge storage unit between a control gate and a channel region defined by a source and a drain, providing a bit line switchably coupled to the drain of each unit and a word line coupled to all the control gates of said page of memory storage units Bit line Precharge 410 Applying an initial, first predetermined voltage to the bit lines of designated memory storage units of the page to enable programming 420 Applying an initial, second predetermined voltage to the bit lines of undesignated memory storage units of the page to be program inhibited Floating the program-enabled bit lines, while raising the programinhibited bit lines from said second predetermined voltage by a 430 predetermined voltage difference to a third predetermined voltage. wherein a predetermined portion of the predetermined voltage difference is coupled as an offset to any neighboring, floated, program-enabled bit lines, and said third predetermined voltage enables floating of the channel of each program-inhibited memory storage unit Program Pulsing, Verifying & Inhibiting Applying a programming voltage pulse to the word line in order to program the designated memory storage units of the page, wherein 440 those un-designated memory storage units of the page are programinhibited by virtue of their floated channel boosted to a program inhibited voltage condition, and a perturbation resulted from the boosting on any neighboring program-enabled memory storage units is compensated by said offset 450 Verifying the designated memory storage units under programming to have been programmed to their target states 460 Re-designating any memory storage units that have not been verified 470 Are all memory storage units of the page verified? Yes 480 **END**

FIG. 10

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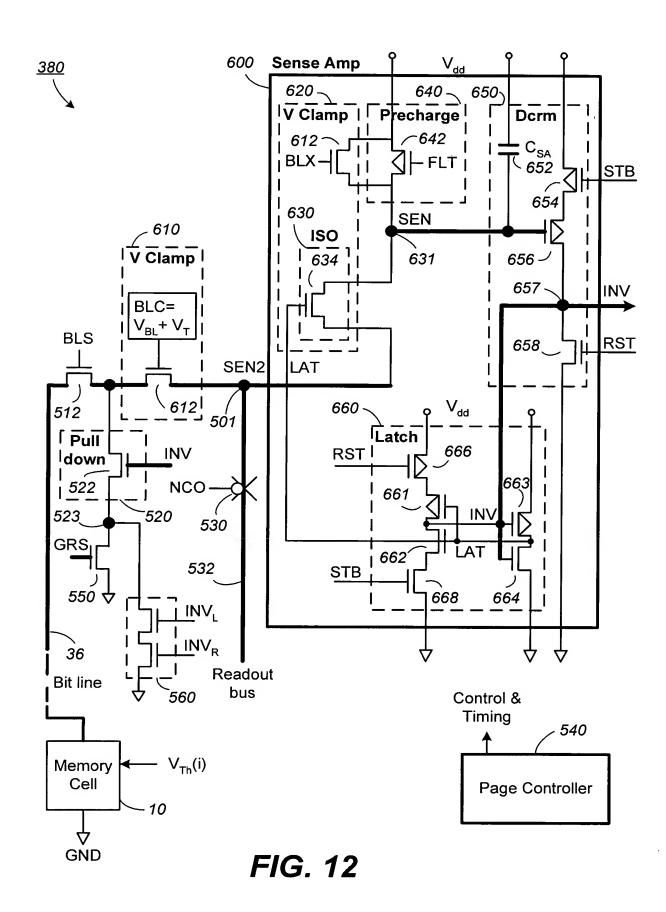
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Bit line Precharge (2nd Embodiment)

Applying an initial, first predetermined voltage to the bit lines of designated memory storage units of the page to enable programming	410'
Applying an initial, second predetermined voltage to the bit lines of undesignated memory storage units of the page to be program inhibited, said second predetermined voltage enables floating of the bit line and channel of each program-inhibited memory storage unit	420'
Floating the program-enabled bit lines, while raising the program-inhibited bit lines from said second predetermined voltage by a predetermined voltage difference to a third predetermined voltage, wherein a predetermined portion of the predetermined voltage difference is coupled as an offset to any neighboring, floated, program-enabled bit lines, and said third predetermined voltage enables floating of the channel of each program-inhibited memory storage unit	430'

FIG. 11



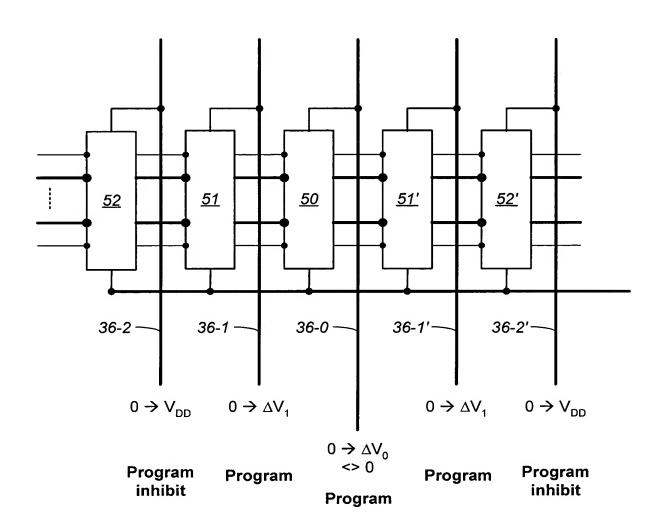


FIG. 13

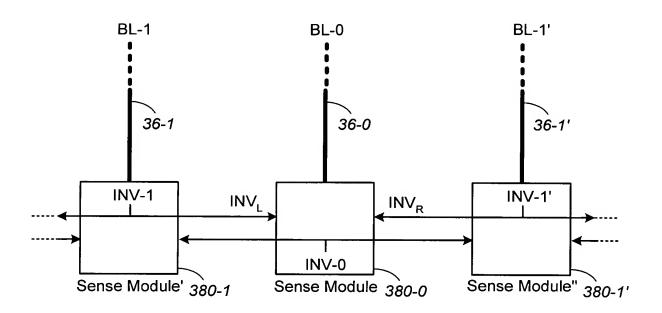


FIG. 14

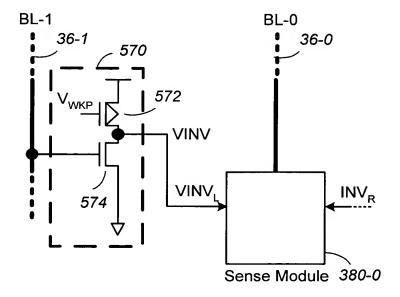


FIG. 15